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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,866	08/31/2001	Michinobu Mizumura	16869P-031900US	2789
20350	7590	09/22/2004	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			NGUYEN, HOAN C	
		ART UNIT		PAPER NUMBER
				2871

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/944,866	MIZUMURA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on \_\_\_\_.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-15 is/are pending in the application.  
4a) Of the above claim(s) 8-12 is/are withdrawn from consideration.  
5)  Claim(s) \_\_\_\_\_ is/are allowed.  
6)  Claim(s) 1-7 and 13-15 is/are rejected.  
7)  Claim(s) \_\_\_\_\_ is/are objected to.  
8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date .

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_ .

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election of Group I (claims 1-7 and 13-15) in the reply filed on 21 June 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 8-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without traverse** in the reply filed on 21 June 2004.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5, 7 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US2001/0035920).

In regard to claims 1, 4 and 13-15, Choi teaches (Figs. 4A-9) a method for repairing line pattern defects comprising steps for

- detecting a shorting defect between a scan line and signal line;
- identifying the location of the defect in a flat panel display unit wherein the scan lines or signal lines or both scan lines and signal lines branch in two parts at an intersection between scan lines and signal lines, disposed with an interlayer insulation film therebetween;
- forming an insulating layer (passivation layer 26) to cover a region at the location of the shorting defect;
- cutting the portion containing the intersection between the scan line and signal line where the shorting defect is located with a laser beam;
- forming an insulation film 51/51a locally at the cut to repair the shorting defect;

where

Claim 2:

- the flat panel unit is a liquid crystal display panel.

Claims 3 and 5:

- heat curing inherently by laser the locally supplied insulation film material for melting insulation film material into cutting regions (paragraph 64<sup>th</sup>).

Claim 7:

- scan lines and signal lines are formed with an interlayer insulation (gate insulating layer 22) film there-between

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US2001/0035920) as applied to claims 1-5, 7 and 13-15 in view of Takizawa (JP363150675A).

Choi fails to disclose a method for repairing line defects in which a shorting defect between a scan line and signal line is detected by applying a voltage between the scan line and signal line and locating a source of infrared detector heat produced at the shorting defect.

Takizawa teaches a method for repairing line defects in which a shorting defect between a scan line and signal line is detected by applying a voltage between the scan line and signal line and locating a source of infrared detector heat produced at the shorting defect for easily and accurately detecting the short-circuit position.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a method for repairing line defects as Choi disclosed, in which a shorting defect between a scan line and signal line is detected by applying a voltage between the scan line and signal line and locating a

source of infrared detector heat produced at the shorting defect for easily and accurately detecting the short-circuit position as taught by Takizawa.

3. Claims 1-5, 7 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salisbury (US5303074A) in view of Interrante et al. (US5193732A).

In regard to claims 1, 4 and 13-15, Salisbury teaches (Fig. 2B, abstract and col. 42 to col. 8 line 3) a method for repairing line pattern defects comprising:

- detecting a shorting defect between a scan line and signal line and
- identifying the location of the defect in a flat panel display unit wherein the scan lines or signal lines or both scan lines and signal lines branch in two parts at an intersection between scan lines and signal lines,
- disposed with an interlayer insulation film therebetween;
- cutting the portion containing the intersection between the scan line and signal line where the shorting defect is located with a laser beam;
- forming an insulation film locally at the cut to repair the shorting defect (col. 7 line 65 to col. 8 line 3).

Claim 2:

- the flat panel unit is a liquid crystal display panel.

Claims 3 and 5:

- heat curing inherently by the locally supplied insulation film material for melting insulation film material into cutting regions.

Claim 7:

- scan lines and signal lines are formed with an interlayer insulation (gate insulating layer) film there-between

However, Salisbury fails to disclose a method for repairing line pattern defects comprising forming an insulating layer to cover a region at the location of the shorting defect.

Interrante et al. teach (Fig. 1A-F) a common way of repairing the defect of a conductive thin film line comprising an insulating layer (polyimide or dielectric insulator layer 28) to cover a region at the location of the shorting defect for protecting coating.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a method for repairing line defects as Salisbury disclosed with an insulating layer to cover a region at the location of the shorting defect for protecting coating as taught by Interrante (col. 8 lines 34-36).

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salisbury (US5303074A) in view of Interrante et al. (US5193732A) as applied to claims 1-5, 7 and 13-15 and in further view of Takizawa (JP363150675A).

Salisbury and Interrante et al. fail to disclose a method for repairing line defects in which a shorting defect between a scan line and signal line is detected by applying a

voltage between the scan line and signal line and locating a source of infrared detector heat produced at the shorting defect.

Takizawa teaches a method for repairing line defects in which a shorting defect between a scan line and signal line is detected by applying a voltage between the scan line and signal line and locating a source of infrared detector heat produced at the shorting defect for easily and accurately detecting the short-circuit position.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a method for repairing line defects as Salisbury disclosed, in which a shorting defect between a scan line and signal line is detected by applying a voltage between the scan line and signal line and locating a source of infrared detector heat produced at the shorting defect for easily and accurately detecting the short-circuit position as taught by Takizawa.

### ***Conclusion***

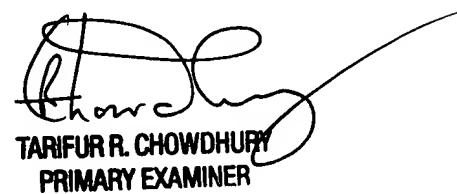
Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN  
Examiner  
Art Unit 2871

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TARIFUR R. CHOWDHURY  
PRIMARY EXAMINER